CIRCUIT OUTPUT STAGE PROTECTION SYSTEM

ABSTRACT OF THE DISCLOSURE

An output stage protection system for protecting CMOS devices in an integrated circuit (IC) output stage during normal operations and power up/power down. In an embodiment, the output stage includes a pair of relatively low voltage CMOS devices coupled to a current source and IC core outputs. A first pair of relatively high voltage CMOS devices is coupled to the relatively low voltage pair and a biasing circuit. A second pair of relatively high voltage CMOS devices is coupled to a resistor, the first pair, and first and second output nodes, respectively. One or more diodes are coupled in series between the first and second output nodes and the resistor. In an embodiment, the output stage protection system protects CMOS devices in the output stage from electrostatic discharge (ESD). Input/output (I/O) pad ESD protection circuits are coupled to the I/O pads and include a clamp coupled to a local net.